REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated April 13, 2007, has been received and its contents carefully reviewed.

Claims 1-3, 5 and 6 are rejected by the Examiner. Claims 1-3, 5 and 6 remain pending in this application.

In the Office Action, claims 5 and 6 are objected to because of informalities. Applicants amend the claims 5 and 6 to be dependent on the Claim 1, as the Examiner suggested.

In the Office Action, claims 1, 2 and 5-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,380,559B1 to Park et al. (hereinafter "Park") in view of U.S. Patent No. 6,429,057B1 to Hong et al. (hereinafter "Hong") and further in view of U.S. Patent No. 5,517,342 to Kim et al. (hereinafter "Kim"). Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Park, Hong and Kim and further in view of U.S. Patent No. 6,255,130B1 to Kim et al. (hereinafter "Kim 130").

The rejection of claims 1-3, 5 and 6 is respectfully traversed and reconsideration is requested. Claims 1-3, 5 and 6 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, "preparing a cutting-off plate having an opening region overlapped with the pad part of the substrate and a cutting-off region overlapped with a remainder part other than the pad part of the substrate; arranging the cutting-off plate on the substrate so that the opening region overlaps with the pad part and the cutting-off region overlaps with the remainder part; and exposing all of the gate pad and the data pad protection electrode of the pad part by a etching process using the cutting-off plate". None of the cited references including Park and Kim singly or in combination, teaches or suggests at least this feature of the claimed invention. The fabricating method of claim 1 of the present invention is different from the Park and Kim fabricating methods in that the photolithographic mask process of Park is not "preparing a cutting-off plate having ...; arranging the cutting-off plate on the substrate ...; and exposing all of the gate pad and the data pad protection electrode..." as recited in claim 1. Accordingly, Applicant respectfully submits that claim 1 and claims 2-3, 5 and 6, which depend from claim 1, are allowable over the cited references.

In addition, the fabricating method of the present invention is to use a cutting-plate as a mask for etching out the whole of the passivation layer and the gate insulating layer covering the gate pad and data pad protection electrode, and this invention does not use photolithographic mask process. As a result, the present invention suggests a method in which the tack time and cost required for performing photolithographic mask processing are reduced remarkably. According to the present invention, the number of photolithographic mask processes is just 3. However, the cited references, Kim, Hong, Park and Kim 130, only teaching about the photolithographic mask processing. The photolithographic mask process generally includes steps of "depositing photoresist on the film, preparing a photo-mask, aligning the photo-mask on the photoresist, exposing the photoresist thorough the photo-mask, developing the photoresist to have the photoresist the same pattern with the mask, etching the film, and removing the photoresist." As so, there are many steps and many materials required in the photolithographic mask process. However, the present invention includes the steps of "preparing a cutting-off plate having ...; arranging the cutting-off plate on the substrate ...; and exposing whole of the gate pad and the data pad protection electrode of the pad part by a etching process using the cutting-off plate." As so, the present invention suggests simplified steps for exposing the gate and data pad.

Furthermore, the photolithographic mask process is used for forming very precise patterns. Therefore, when each (gate and data) pad has its own pad hole, the photolithographic mask process should be used. However, the method of the present invention is applied for forming rough patterns. As so, in the present invention, each pad has its own pad hole but the whole pad area is exposed by etching out the passivation layer and gate insulating layer covering the (gate and data) pads. As a result, the claim recites a combination of elements including, for example, "exposing all of the gate pad and the data pad protection electrode of the pad part by a etching process using the cutting-off plate" that is not taught by any of the cited references and by any combination of them.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. *A duplicate copy of this sheet is enclosed.*

Respectfully submitted,

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